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PATENT APPLICATION
Attorney's Docket No. 1482-138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Barrie Gilbert

Serial No. 09/694,731 Examiner: Quan Tra

Filed: October 23, 2000 Group Art Unit: 2816

For: LOW SUPPLY CURRENT RMS-TO-DC CONVERTER

Date: September 5, 2003

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

This Appeal Brief is in furtherance of the Notice of Appeal mailed in this case on May 5, 2003. Appeal is taken from the Examiner's Office Action mailed November 5, 2002 rejecting claims 1, 3, 5-7 and 15.

Also enclosed is:

☒ Form PTO-2038 authorizing payment in the amount of $730.00 for the appeal brief fee ($320.00) and the two-month extension fee ($410.00) – large entity

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Respectfully submitted,

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FOR TRADEMARKS 2800 CRYSTAL DRIVE ARLINGTON, VA 22202-3513

ON: 9-05-03
Christina Lawton

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Attorney's Do. No. 1482-138

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The fees required under §1.17(c) and any required petition for extension of time for filing this Brief and fees therefor are submitted with the accompanying TRANSMITTAL OF APPEAL BRIEF.

This Brief is submitted in triplicate.

REAL PARTY IN INTEREST

The present application has been assigned to the following party:

Analog Devices, Inc.
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Norwood, MA 02062-9106

RELATED APPEALS AND INTERFERENCES

The Board's decision in the present Appeal will not directly affect, or be directly affected, or have any bearing on any other appeals or interferences known to the appellant, or to the Applicant's legal representative.

STATUS OF CLAIMS

Claims in the application: 1, 3-12, 14 and 15

Claims allowed: 8-12 and 14

Claims allowable if rewritten in independent form: 4

Claims rejected: 1, 3, 5-7 and 15

Claims appealed: 1, 3, 5-7 and 15

STATUS OF AMENDMENTS AND APPEALS

This is the second Appeal Brief filed by Applicant in this case. The first Appeal Brief was filed on September 3, 2002. Rather than filing an Examiner's Response, however, the Examiner issued a non-final Office Action dated November 5, 2002 (paper no. 12) setting forth new grounds of rejection of claims 1, 3, 5-7 and 15.

Applicant hereby appeals the decision of the Primary Examiner mailed November 5, 2002 (paper no. 12) rejecting claims 1, 3, 5-7 and 15. Although the current rejection is non-final, these claims were also rejected in an Office Action mailed March 13, 2002. 37 CFR 1.191(a).

SUMMARY

The claims on appeal relate to squaring cells which are used to generate an output signal that is equal to the mathematical square of an input signal applied to the cell. The particular squaring cells at issue provide a good mathematical square-law approximation over a limited input signal range (that is, when the input signal is below a certain value). If the input signal becomes too large, the square-law approximation begins to break down, and the squaring cell loses accuracy. The range of input signals over which the squaring cell maintains its accuracy is related to the steady-state current (also called the "quiescent" or "bias" current) through the cell (see page 4 of the specification at lines 28-29.

ISSUES ON APPEAL

Whether claims 1, 3, 5-7 and 15 are unpatentable under 35 U.S.C. 103(a) as being obvious in view of U.S. Patent No. 4,250,457 to Hofmann ("Hofmann").

GROUPING OF CLAIMS

Claims 1, 3, 5-7 and 15 stand together for purposes of this appeal.

ARGUMENT

Claims 1, 3, 5-7 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,250,457 to Hofmann ("Hofmann").

Claim 1 recites a method for operating a squaring cell and includes the limitation of "limiting the input signal to a range in which the output function of the transistor cell approximates a square-law." As discussed above in the summary, the square-law approximation of the squaring cell begins to break down when the input signal becomes too large. Thus, the desirability of limiting the input signal. Hofmann does not disclose or suggest limiting the input signal in any way. In fact, as will be discussed below, Hofmann actually discloses the desirability of using a large input signal to achieve a linear response, thereby *avoiding* a square-law response.

In rejecting claim 1 the Examiner acknowledges that Hofmann does not disclose limiting the input signal, but then concludes that, because Hofmann's circuit "is usable to provide a square law" (Paper no. 2, Office Action page 2), is would have been obvious to limit the input signal to a range that provides such a response. In essence, the Examiner argues that, because the circuit disclosed in Hofmann is capable of being operated as recited in claim 1, it would have been obvious to do so. But just because a prior art apparatus is *capable* of being operated as claimed by applicant would not have made it *obvious* to do so. It is axiomatic that an applicant can claim a new and nonobvious method for operating a prior art apparatus.

In support of the obviousness rejection, the Examiner points to the presence of an equation at col. 5, lines 15-18 of Hofmann. The Examiner then goes on to state that Hofmann's equation teaches that "when the input signal is relatively small, the cell substantially provides a square-law, and when the input signal is relatively large, the cell provides a linear function" (Paper no. 12, Office Action page 2). But Hofmann does not explain these two modes of operation, nor does it disclose or suggest limiting the input signal to a range in which the output function of the transistor cell approximates a square-law as recited in claim 1. Significantly, the Examiner did not point out these two modes of operation until after it was explained at page 3 of Applicant's first Appeal Brief.

It took the Applicant's disclosure to identify these modes of operation, and then teach limiting the input signal to a range that would approximate a square law. The equation at

col. 5, lines 15-18 of Hofmann is essentially the same as Eq. 1 at page 4, line 10 of Applicant's specification, except for minor differences in notation. Applicant's specification explains that the squaring cells have two distinct modes of operation. If the input signal applied to the squaring cell is limited to less than about ±4 times the bias current, the squaring cell provides a good square-law approximation. That is, the operation of the squaring cell is limited to the curved (i.e., nonlinear) portion of the solid curve shown in Fig. 2 of Applicant's specification. (See the specification at page 4, lines 8-22 and page 4, line 28 - page 5, line 2.) If, however, the input signal is relatively large, the output is approximately equal to the absolute-value of the input signal; that is, the output of the cell becomes a linear function which is shown in Applicant's Fig. 2 as a broken line for comparison. (See the specification at page 4, lines 23-27.)

The entire thrust of Hofmann is to achieve a linear operating characteristic. (See, e.g., col. 1, lines 8, 15 and 17; col. 2, line 46; col. 4, lines 7-9; col. 5, lines 19-21; col. 6, lines 3 and 14; etc., all emphasizing the desirability of achieving high linearity.) At col. 5, lines 19-21, Hofmann expressly states the advantage of making the input signal (I_{in}) much larger than the bias current (I_b) for the purpose of achieving a linear output. This is in contrast to claim 1 which recites limiting the input signal to a specific range that provides a square-law characteristic. Thus, Hofmann actually teaches away from the claimed invention.

Hofmann's only hint of nonlinear operation is at col. 5, lines 21-25 where it mentions that the detector might be useful for applications where it is desirable to generate a signal corresponding to the square root of the sum of the square of two inputs. But this is far from the simple square law approximation recited in claim 1, and there is no suggestion or motivation to limit the input signal in any way as recited in claim 1.

Claim 15 recites a method for operating a squaring cell in which the input signal is limited to less than about four times the bias current. At page 3 of Paper no. 12, Office Action, the Examiner acknowledges that Hofmann does not teach this limitation, but then argues that this selection of current range would have been an obvious "design choice" depending upon the particular environment of use to ensure optimum performance. This argument, however, is based on the faulty assumption that Hofmann actually teaches limiting the input signal range. It cannot be obvious to select a specific input signal range when the prior art does not teach limiting the input signal to *any* range.

CONCLUSION

Applicant requests that the rejection of claims 1, 3, 5-7 and 15 be reversed.

Respectfully submitted,

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ON 9/5/03
Christina Lawton

APPENDIX

The claims of the present application read as follows:

1. A method for operating a transistor cell comprising an input terminal for receiving an input signal, an output terminal for transmitting an output signal, a grounded base transistor coupled between the input and output terminals, and a current mirror coupled between the input and output terminals, the method comprising:

biasing the transistor cell to establish a bias current in the grounded base transistor and the current mirror when the input signal is zero; and

limiting the input signal to a range in which the output function of the transistor cell approximates a square-law.

2. (Cancelled)

3. A method according to claim 1 further including adjusting the bias current, thereby adjusting the input impedance of the cell.

4. A method according to claim 1 wherein biasing the transistor cell includes:

coupling a bias signal to the base of the grounded base transistor; and

varying the bias signal with temperature such that it causes the bias current through the grounded base transistor and the current mirror to be proportional to absolute temperature.

5. A method according to claim 1 wherein:

the current mirror is coupled to a power supply terminal; and

biasing the transistor cell includes maintaining the base of the grounded base transistor at about $2V_{BE}$ from the voltage of the power supply terminal.

6. A method according to claim 1 further including isolating the current mirror from the output terminal.

7. A method according to claim 6 wherein isolating the current mirror includes coupling a cascode transistor between the output terminal and the current mirror.

8. A squaring cell comprising:

an input terminal;

an output terminal;

a grounded base transistor coupled between the input and output terminals;

a current mirror coupled between the input and output terminals; and

a bias signal generator coupled to the grounded base transistor to establish a bias current through the grounded base transistor and the current mirror, wherein the bias signal generator generates a bias signal that varies with temperature such that it causes the bias current through each of the transistors to be proportional to absolute temperature.

9. A squaring cell according to claim 8 further including a cascode transistor coupled between the current mirror and the output terminal.

10. A squaring cell according to claim 8 wherein the current mirror is coupled to a power supply terminal, and the bias signal generator maintains the base of the grounded base transistor at about $2V_{BE}$ from the voltage of the power supply terminal.

11. A squaring cell according to claim 8 wherein the current mirror includes:

a diode-connected transistor coupled between the input terminal and a power supply terminal; and

a mirror transistor having a collector coupled to the output terminal, a base coupled to the input terminal, and an emitter coupled to the power supply terminal.

12. A squaring cell according to claim 8 wherein:

the grounded base transistor has a collector coupled to the output terminal, a base for receiving the bias signal, and an emitter coupled to the input terminal;

the current mirror includes:

a diode-connected transistor having a collector and base coupled to the input terminal and an emitter coupled to a power supply terminal, and

a mirror transistor having a collector coupled to the output terminal, a base coupled to the input terminal, and an emitter coupled to the power supply terminal.

13. (Cancelled)

14. A squaring cell according to claim 8 wherein the bias signal generator includes:

two diode-connected transistors coupled in series between the input terminal and a power supply terminal; and

a current source coupled to the diode connected transistors to cause a bias current to flow through the diode connected transistors.

15. A method according to claim 1 wherein limiting the input signal to a range in which the output function of the transistor cell approximates a square-law comprises limiting the input signal to less than about four times the bias current.